**AMENDMENTS TO THE CLAIMS:**

This listing of claims will replace all prior versions and listings of claims in the application:

1-12. (Cancelled)

13. (Previously Presented) A method for fabricating a semiconductor transistor, comprising:

forming an LDD region using an ion implantation in a substrate;

forming a first insulating layer on the substrate;

patterning the first insulating layer;

forming a trench in the substrate;

forming a trench gate by depositing and planarizing a second insulating layer and a conductor on the substrate with the trench formed therein, the trench gate comprising the second insulating layer and the conductor;

anisotropically etching the first insulating layer to form spacers; and

forming source/drain regions by performing an ion implantation on the substrate using the spacers and the trench gate as a mask.

14. (Original) The method of claim 13, further comprising performing a thermal process after forming the source/drain regions.

15. (Original) The method of claim 13, wherein the first insulating layer is an oxide layer or a nitride layer.

16. (Original) The method of claim 13, wherein the conductor comprises one selected from the group consisting of polysilicon, tungsten alloys, titanium alloys, and tantalum alloys.

17. (Original) The method of claim 13, wherein the energy of the ion implantation for forming the LDD region is between 10 keV and 80 keV.

18. (Original) The method of claim 13, wherein the energy of the ion implantation for forming the source/drain regions is between 10 keV and 100 keV.

19. (Original) The method of claim 13, wherein the trench is formed by dry etching.

20. (Original) The method of claim 13, wherein the trench is formed by a dry etching using an angle etching and chemical dry etching.

21. (Original) The method of claim 20, wherein lower edges of the trench are formed in a rounded shape.

22. (Original) The method of claim 20, wherein the chemical dry etching uses $CF_4/O_2$ or $CHF_3/O_2$.

23. (Original) The method of claim 13, wherein planarizing a second insulating layer and a conductor comprises a CMP process using the first insulating layer as an etch-stop layer.

24-31. (Cancelled)